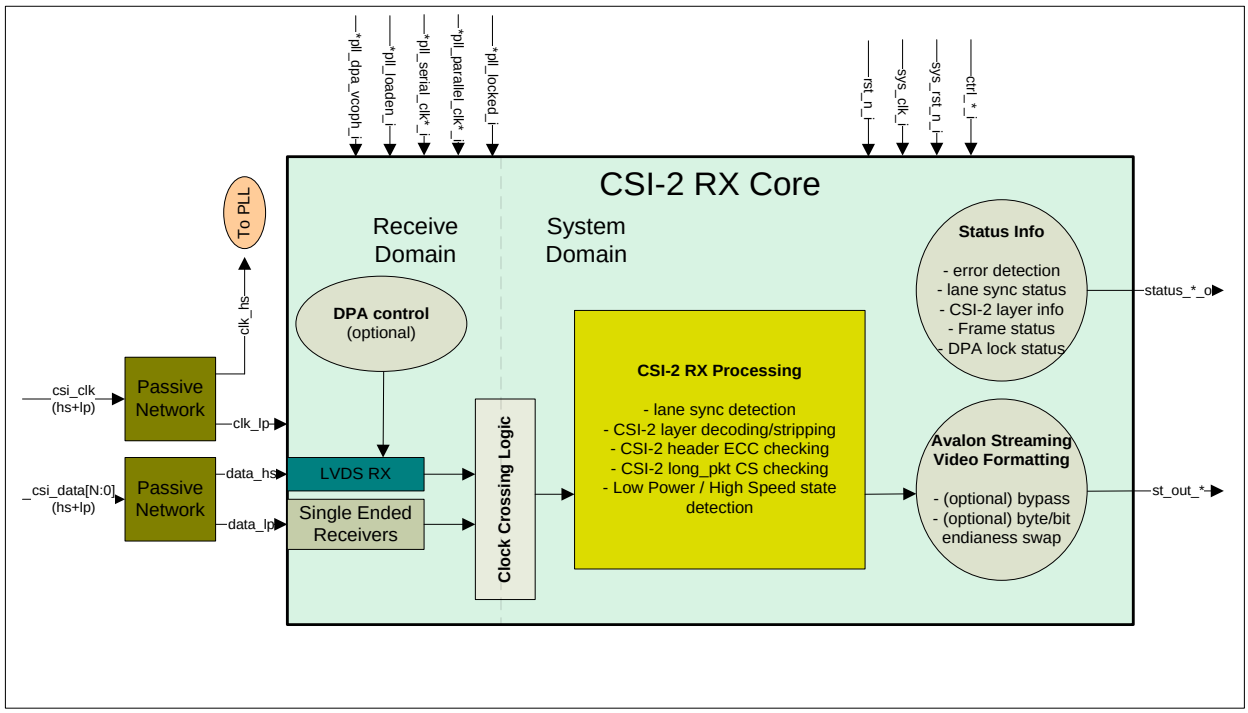
FORESYS

CSI-2 Rx Core

Description

The Foresys CSI-2 RX Core provides a fast path to integrating Image Sensors into a wide variety of products based on Intel FPGA devices. It is designed to convert CSI-2 encoded data from an image sensor into an Avalon Streaming Video interface.



Base Features

- ✓ Provides Compatible D-Phy v1.1 physical layer using FPGA LVDS/LVCMOS IO and passive network.
- ✓ Supports CSI-2 protocol for unidirectional data transfer.
- ✓ Compatible with D-PHY Configured for 1 clock and {1,2, or 4} data lanes.
- ✓ Intended for per-lane clocks rates up to 1.5 Gbps, depending on device speed grade.
- ✓ Supports multiple FPGA families (including Arria10, Cyclone10, CycloneV, and Max10).
- ✓ Supports up to 4 Virtual Channels.
- ✓ Optional Dynamic Phase Alignment (DPA) control for LVDS RX data.
- ✓ Provides per-lane sync status.
- ✓ Provides error detection info including:
  - Lane sync error detection.
  - CSI-2 header ECC error detection.
  - CSI-2 long_pkt footer CS error detection.
  - Frame SOF/EOF error detection.
  - Frame SOL/EOL error detection.
- ✓ Provides CSI-2 layer info.
- ✓ Transmits Avalon ST Video format.

Optional Extended Features

Foresys can provide a customized CSI-2 Core including:

- ✓ Link performance data including:
  - SOF message count
  - EOF message count
  - Data message count
  - ECC uncorrected error count
  - CRC error count
- ✓ Conversion to specific video formats
- ✓ Corrections of single bit ECC errors
- ✓ Support for other Intel FPGA families
- ✓ Optional animated test pattern generator
- ✓ Support for intelligent flow control handling

Please contact Foresys at ip@foresys.com for more information on customization options.

Core Details

The Core will function in most Intel FPGA Devices, but requires customization given the PLL and IO resources available within the selected parts. Please contact Foresys at ip@foresys.com for more information on pricing and customization options.

Fabric Resources (Max10)

	Logic Elements	M9Ks	PLLs
Base Functionality (1 Lane)[1]	850	1	1
Base Functionality (2 Lanes)[1]	960	1	1
Base Functionality (4 Lanes)[1]	1320	1	1

[1] Features listed as "Extended Features" may require additional logic cells to implement

Example Application

This is a simple example of a Max 10 being used to process image data being received by a CSI-2 camera and passing the resultant image data back out a CSI-2 TX interface.