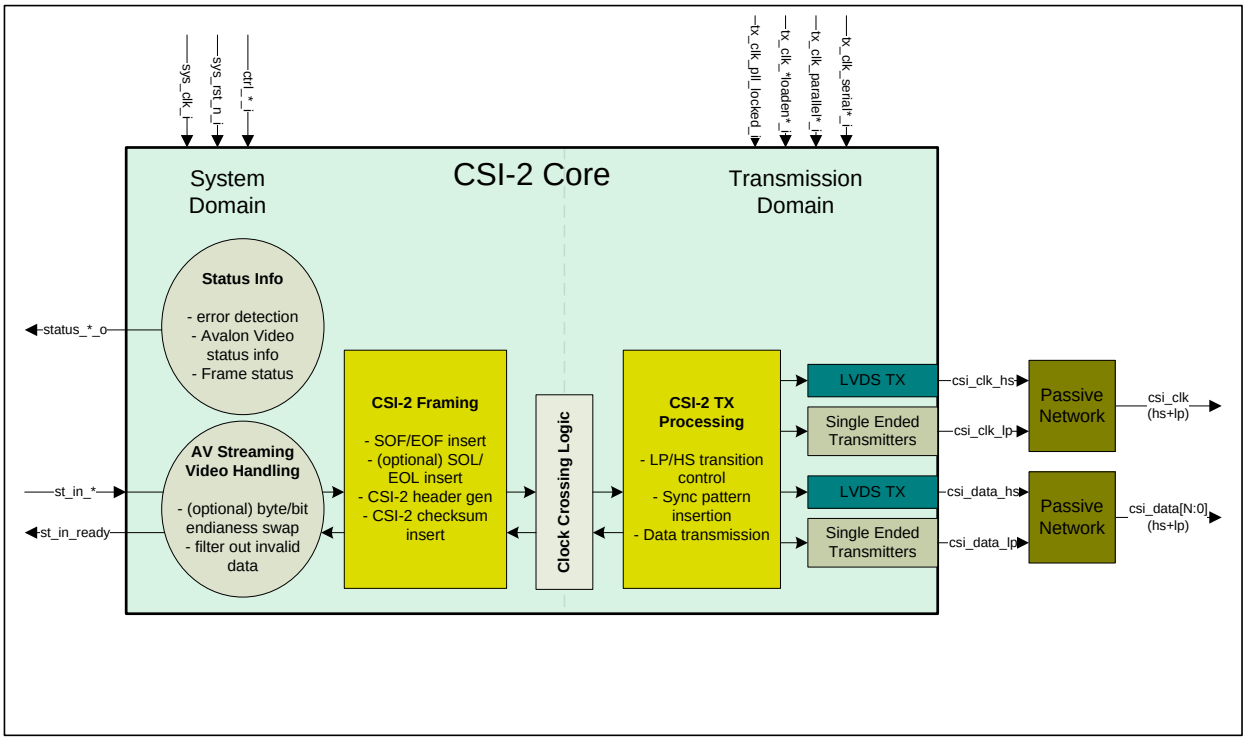
FORESYS

CSI-2 Tx Core

Description

The Foresys CSI-2 TX Core provides a fast path to integrating Image Sensors into a wide variety of products based on Intel FPGA devices. It is designed to convert an internal payload agnostic Avalon Streaming data bus to CSI-2 data.



Base Features

- ✓ Provides Compatible D-Phy v1.1 physical layer using FPGA LVDS/LVCMOS IO and passive network.
- ✓ Supports CSI-2 protocol for unidirectional data transfer.
- ✓ Compatible with D-PHY Configured for 1 clock and {1,2, or 4} data lanes.
- ✓ Intended for per-lane clocks rates up to 1.5 Gbps, depending on device and speed grade.
- ✓ Processes incoming standard Avalon Streaming Video Packets.
- ✓ Supports {Arria10, Cyclone10, CycloneV, Max10}
- ✓ Supports up to 4 Virtual Channels with CSI-2 encapsulation, including:
  - CSI-2 short_pkt insert [SOF,EOF]
  - CSI-2 short_pkt insert [SOL,EOL] (optional)
  - CSI-2 header and ECC field.
  - CSI-2 long_pkt footer CS field.
- ✓ Transmits CSI-2 Packets including: LP to HS state transition, sync pattern, payload, and trailer.
- ✓ Provides error detection info including:
  - pre_fifo and dc_fifo overflow/underflow.

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Optional Extended Features

Foresys can provide a customized CSI-2 Core including:

- ✓ Support for other Intel FPGA families
- ✓ Optional test data generator
- ✓ Support for other input packet formats
- ✓ Intelligent flow control and buffer management for multiple CSI-2 Virtual Channels.

Please contact Foresys at ip@foresys.com for more information on customization options.

Core Details

The Core will function in most Intel FPGA Devices, but requires customization given the PLL and IO resources available within the selected parts. Please contact Foresys at ip@foresys.com for more information on pricing and customization options.

Fabric Resources (Max10)

	Logic Elements	M9Ks	PLLs
Base Functionality (1 Lane)[1]	950	3[2]	1[3]
Base Functionality (2 Lanes)[1]	1030	3[2]	1[3]
Base Functionality (4 Lanes)[1]	1060	3[2]	1[3]

[1] Features listed as "Extended Features" may require additional logic cells to implement

[2] The number of M9Ks required depends on architecture specific traffic burst patterns. This number includes one M9K for the CSI-2 insertion FIFO and two M9Ks for traffic to the LVDS transmitters

[3] The core takes clocks generated by an external PLL and does not instantiate a PLL directly. Two clocks are required in addition to a copy of the system datapath clock

Example Application

This is a simple example of a Max 10 being used to process image data being received by a CSI-2 camera and passing the resultant image data back out a CSI-2 TX interface.